

1 (10) ABSTRACT

2 In cellular MOSFET transistor arrays using a geometric gate construction, deleterious
3 inherent capacitance induced by the construction is substantially reduced by the use of
4 plugs in between adjacent source regions of transistor source rows and adjacent drain
5 regions of transistor drain rows of the array. Embodiments using field oxide, thicker step
6 gate oxide, dielectric materials in a floating gate construction, and shallow trench isolation
7 region plugs are described.